Midasmicro

TX56-PAM4

56-Gb/s PAM4 Transmitter

KEY FEATURES

- Data rate ranges up to 56 Gb/s with PAM-4 signal
- Built-in PRBS7 generator
- Duty cycle correction up to 40%-60%
- Programmable pre-emphasis up to 8-dB boosting
- Differential output swing of 600 mV

APPLICATIONS

- SerDes and data link testing for 400GbE

DESCRIPTION

TX56-PAM4 is a high speed transmitter provides high-quality differential data with PAM-4 signal up to 56 Gb/s and beyond. Driven by external quarter-rate clocks (i.e., 14-GHz clock input for 56-Gb/s data output), **TX56-PAM4** generates PAM-4 signal which combines two true pseudo-random bit sequence (PRBS) of length 2^7-1 with built-in PRBS generator, or fed four quarter-rate data sequence from external. **TX56-PAM4** achieves differential output magnitude of 600 mV and a duty cycle correction (DCC) unit provides a maximum tunable range of 40%~60%, well beyond any possible eye distortion.

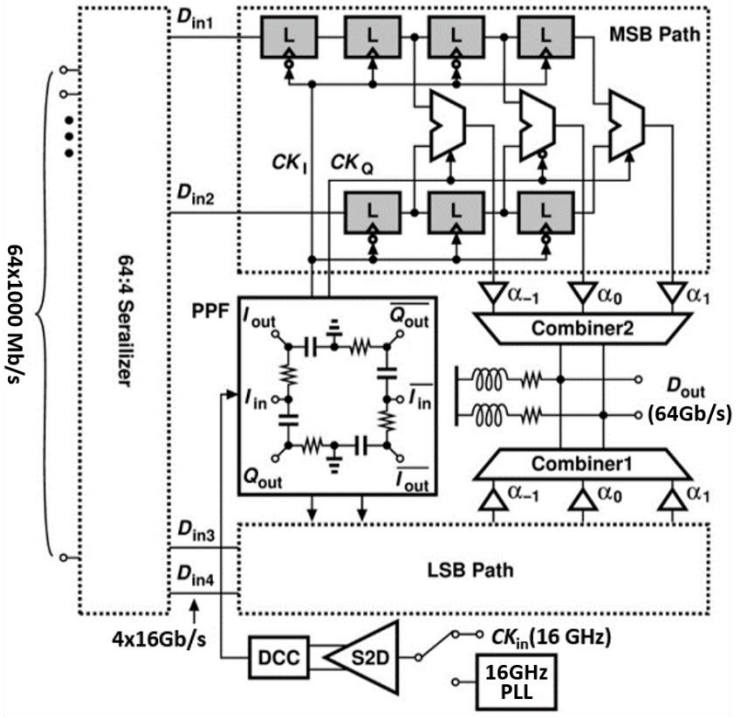

Fig. 1. Functional Block Diagram

SPECIFICATIONS

Table. 1. Spec.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS/NOTES
TX56-PAM4 Overall					
Data Rate			56	Gb/s	
Data Rate Resolution	continuous, depending on clock input				
Function	50Ω output driver, built-in PRBS7 generator, external data/clock input, duty cycle correction, 3-tap feed-forward equalizer(FFE)				
Pattern	Combine two PRBS length of 2^7-1, or fed four quarter-rate data sequence from external				
Supply Voltage		1 1.5		V V	1V for core block 1.5V for output driver.
Total Power Dissipation		200		mW	
Clock Input					
Frequency			14	GHz	1/4 data rate, single-ended
Resolution	continuous, depending on clock input				
Input Power Level	0		16	dBm	Single, ac-coupled, 50-Ω terminated, SMA female
Duty Cycle Correction			40-60	%	5-bit control
Data Input					
Data Rate			14	Gb/s	1/4 data rate, single-ended
input Swing		400		mV_{pp}	Single, ac-coupled, 50-Ω terminated, SMA female
Data Output					
Output Swing		600		mV_{pp}	Differential, ac-coupled, 50-Ω terminated, 1.85mm female
Pre-Emphasis	0		8	dB	3-tap FFE, programmable
Pre-Emphasis Adjust	4-bit coefficient setting				

TYPICAL PERFORMANCE

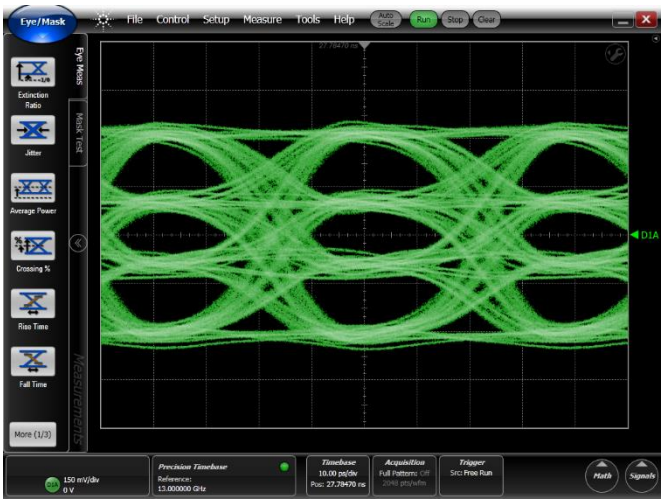

Fig. 2. Data eye at 52 Gb/s, PRBS 2^7-1.

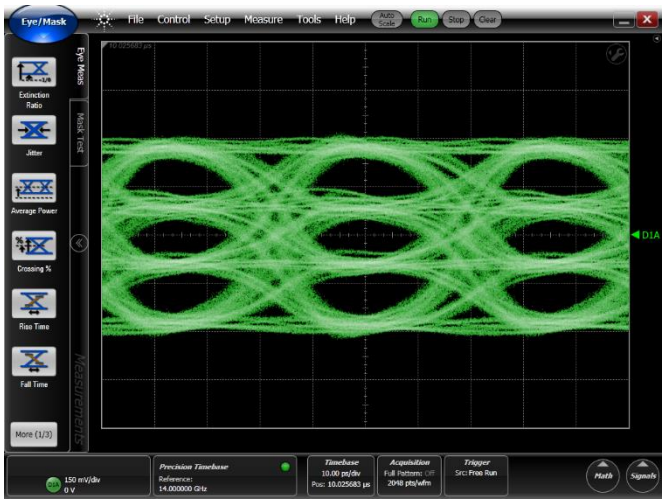

Fig. 3. Data eye at 56 Gb/s, PRBS 2^7-1.

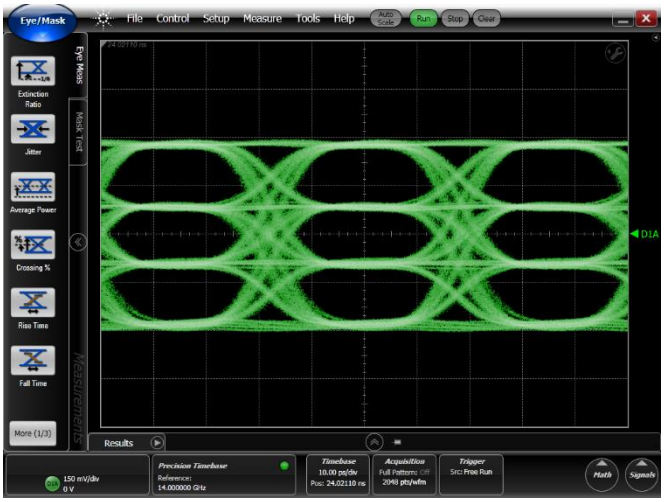

Fig. 4. Probed data eye at 56 Gb/s, PRBS 2^7-1.

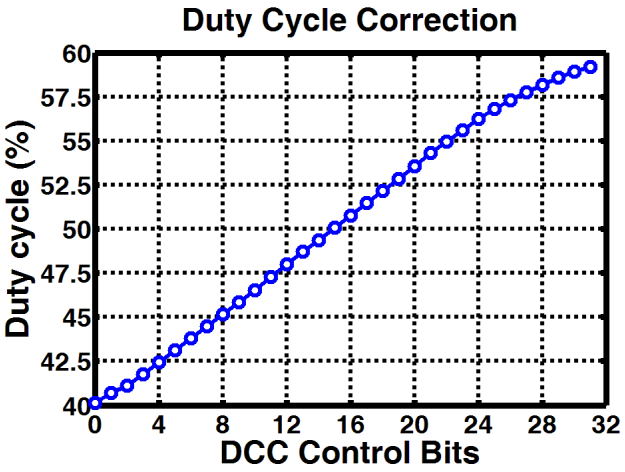

Fig. 5. DCC control.

CHIP PHOTO & PIN CONFIGURATION

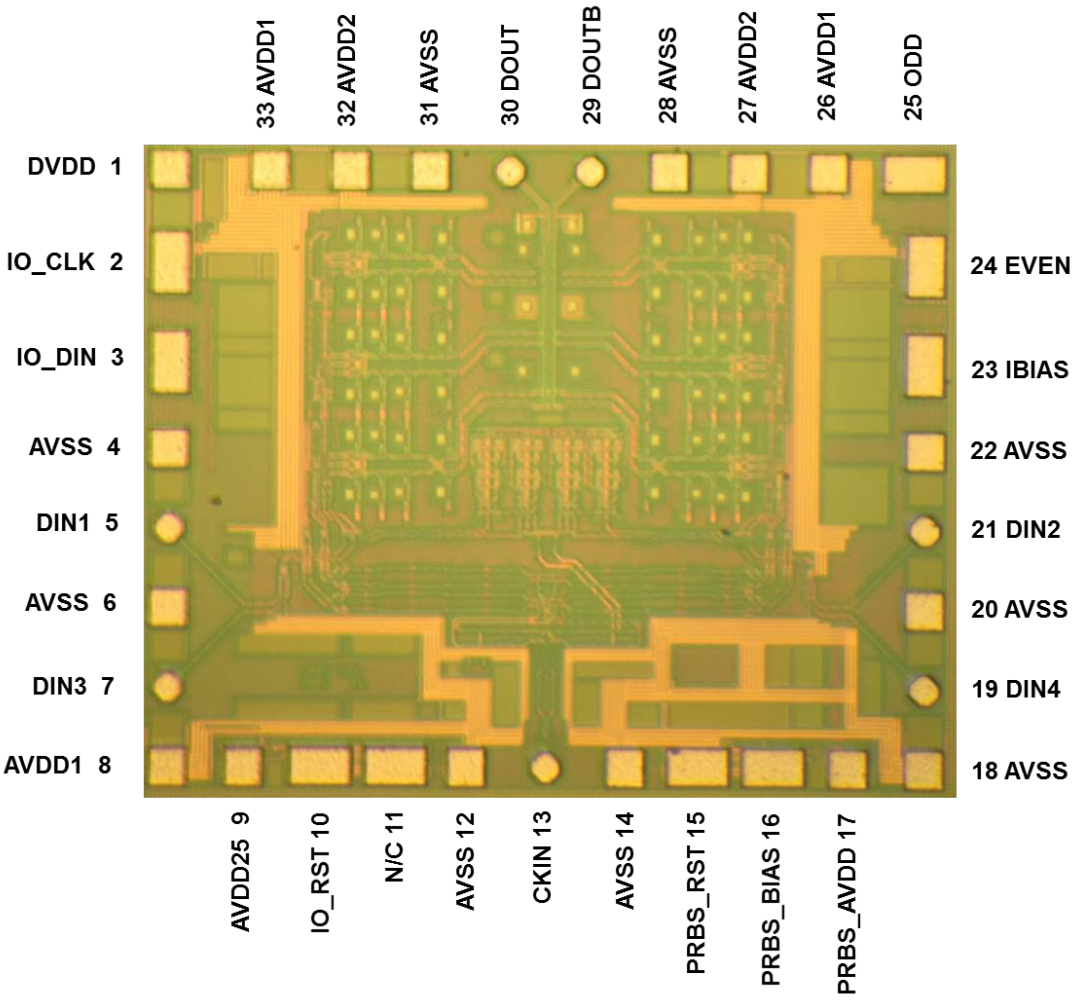

Fig. 7. Pin Configuration

Pin Function Descriptions

Table. 2. Pin Function Descriptions

Pin No.	Name	Description
1	DVDD	Positive power supply for the digital Section. Typical value is 1.2V.
2	IO_CLK	The clock input of Serial Peripheral Interface.
3	IO_DIN	The data input of Serial Peripheral Interface.
4, 6, 8, 12, 14, 18, 20, 22, 28, 31	AVSS	Analog ground.
5,7,19,21	DIN1, DIN2, DIN3, DIN4	External data input (1/4 data rate).
9	AVDD25	Positive power supply for the Band gap reference. Typical value is 2.5V.
10	IO_RST	The reset of Serial Peripheral Interface.
11	N/C	No connection.
13	CKIN	Clock input (1/4 data rate).
15	PRBS_RST	The reset of built-in PRBS generator.
16	PRBS_BIAS	The bias of built-in PRBS generator.
17	PRBS_AVDD	Positive power supply for built-in PRBS generator.
23	IBIAS	Bias of constant IR drop.
24, 25	ODD, EVEN	Analog tuning of DCC.
26, 33	AVDD1	Positive power supply for the core system. Typical value is 1.2V.
27, 32	AVDD2	Positive power supply for the output driver. Typical value is 1.5V.
29, 30	DOUT, DOUTB	Data output.