RX28-NRZ User Manual

General NRZ Receiver 28G

KEY FEATURES

- Wide range input data rate(1~15Gb/s,25,28Gb/s)
- Small input sensitivity < 50 mV (@25Gb/s)
- Wide range programmable output amplitude (300m~930mV_{ppd})
- Output driver with 3-tap FFE provide maximum 8dB boosting
- low power consumption (130mW for Bypass CDR mode,220mW for CDR mode)
- CDR(Clock and Data Recovery circuit) lock time < 10μs
- Supports -20°C to + 100°C temperature range

APPICATIONS

- SerDes and data link testing for 25.78125 Gb/s
- Data center and in-rack connection

DESCRIPTION

The **RX28-NRZ** is a multi-band NRZ receiver with wide input data rate range (1~15Gb/s, 25Gb/s,28Gb/s) and can be applied in typical data link testing. The functional block diagram of RX28-NRZ is shown in Fig. 1. **RX28-NRZ** can operate in "bypass CDR mode" to save power consumption, in which input data can be operated from 1 to 15Gb/s, and can be only processed by front-end circuits and driven by output driver. When operated in "CDR mode", **RX28-NRZ** can automatically detect input data rate (After select 25Gb/s or 28Gb/s mode) to lock the CDR at correct frequency, and finally recovered differential data output is retrieved with magnitude within 300mV to 930mV (programmable by users, without pre-emphasis), peak-to-peak data jitter less than 7 ps.

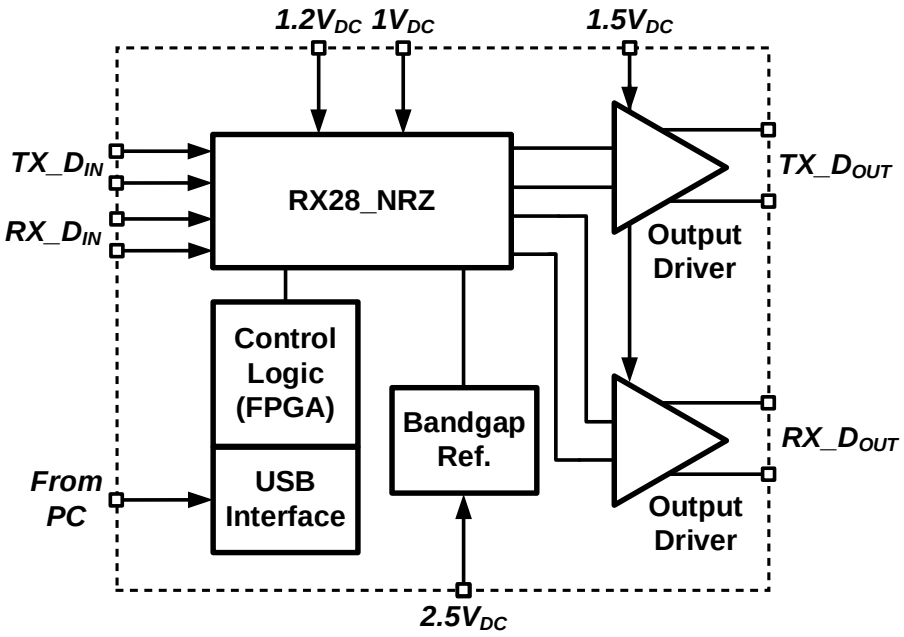

Fig. 1. Functional Block Diagram

SPECIFICATIONS

SYMBOL	PARAMETER	Note	MIN	TYP	MAX	UNIT
RX25-OPT Overall						
VCCR / VCCT	Core supply voltage for RX/TX (CDR/DFE)			1		V
VCCLA	Supply voltage for front-end circuit			1.2		V
VCCDR	Supply voltage for output driver			1.5		V
VCCBG	Supply voltage for bandgap reference			2.5		V
P_{TOTAL}	Power dissipation @ input data rate = 10 Gb/s			130		mW
	Power dissipation @ input data rage = 25 Gb/s			220		mW
Data Input						
DR 25G	Input data rate for bypass CDR mode		1		15	Gb/s
	Input data rate for retime at 25 Gb/s mode		25.5		26	Gb/s
	Input data rate for retime at 28 Gb/s mode		27.5		28.05	Gb/s
V_{in_sense}	Sensitivity at input data rate = 25 Gb/s			50		mV
Data / Clock Output						
V_{OUT_DATA}	Differential data output swing	1	300		930	mV
A_{PRE}	Pre-emphasis, 3-tap FFE, programmable		0		8	dB
$T_{RISE/FALL}$	Output rise/fall time			<13		ps
S_{DD11}	Input differential mode return loss	2		<-10		dB
V_{CM_DATA}	Output data common mode	3	1.035		1.35	V
CDR						
JT_{DATA}	Recovered data jitter @ 25.78125 Gb/s, PRBS31 data			<7.0		ps,pp
				<1.0		ps,rms
JT_{CK}	Recovered clock jitter			<350		fs,rms
T_{LOCK}	CDR lock time			<10		µs
J_{PEAK}	Jitter peaking			<0.1		dB
IJTOL	Input jitter tolerance	4		0.7		UI
RJ	Random jitter w/i CDR			<350		fs,rms
	Random jitter w/o CDR			<1		ps,rms
DJ	Deterministic jitter @ 25 Gb/s			<5		ps,pp
LA & EQ						
A_{LA}	LA gain			20		dB
A_{EQ}	EQ Boosting, programmable		0		9	dB

NOTES:

1. DC-coupled, 50-Ω terminated, 1.85mm female (CML Logic).
2. From 0.01 GHz to 28 GHz
3. Single-ended, DC-coupled, 50-Ω terminated
4. SJ=0.2UI, High-frequency JTOL > 0.2 UI

TYPICAL PERFORMANCE

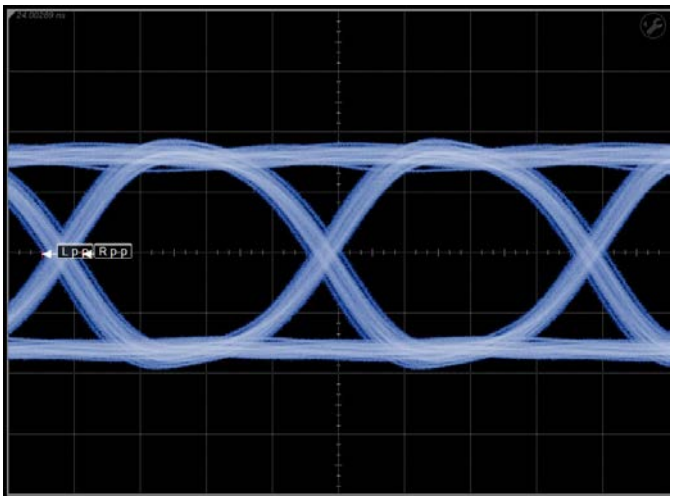

Fig. 2. Output Data Eye at 25 Gb/s, PRBS7

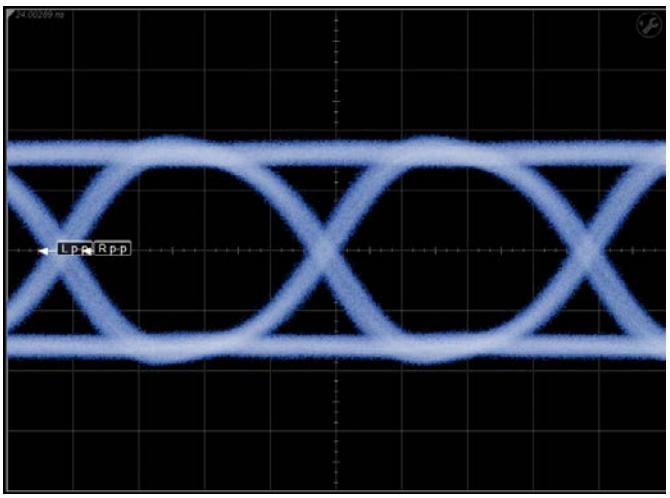

Fig. 3. Output Data Eye at 25 Gb/s, PRBS15

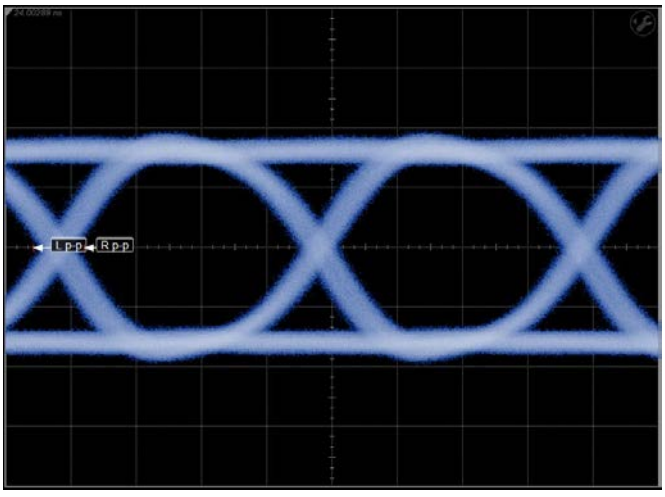

Fig. 4. Output Data Eye at 25 Gb/s, PRBS23

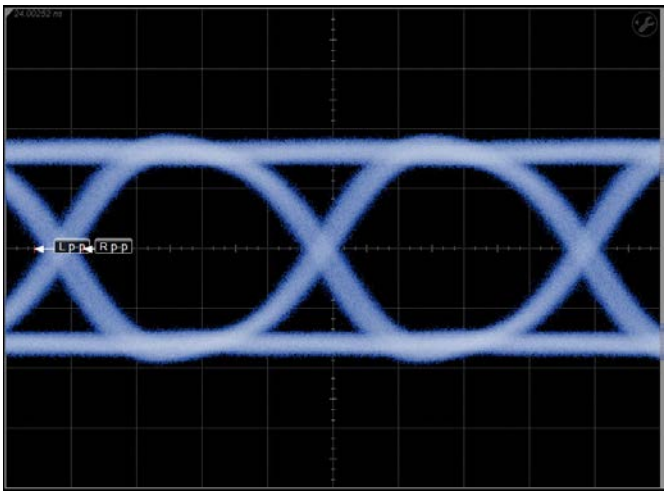

Fig. 5. Output Data Eye at 25 Gb/s, PRBS31

User Guide

SOFTWARE INSTALLATION

The control panel is programmed and compiled by using LabVIEW. If LabVIEW has been installed in your PC, skip Part I. Otherwise, proceed the following software installation sequentially before operation. The software for operation of is **Application.exe** as shown below.

Part I: National Instruments LabVIEW Run-Time Engine (LVRTE2011SP1f2std.exe)

- This execution file can be found in the USB driver. Alternatively, it could be downloaded from National Instruments official website. Follow the instructions on screen. Use the default **Destination Directory** and install all features. Uncheck the option "Request the installer to contact National Instruments...." if you don't need new notifications and updates. Restart your PC after the installation is complete.

Part II: **RX28-NRZ** Control Software (Application.rar)

- Extract Application.rar. The following files will be shown in the list. Run the application file "**Application.exe**".

Fig. 6. Executing Application.exe.

- The software front-panel display appears as illustrated in Fig. 7, followed by the control signal table. The left half part of control panel is for TX and the right half is for RX.

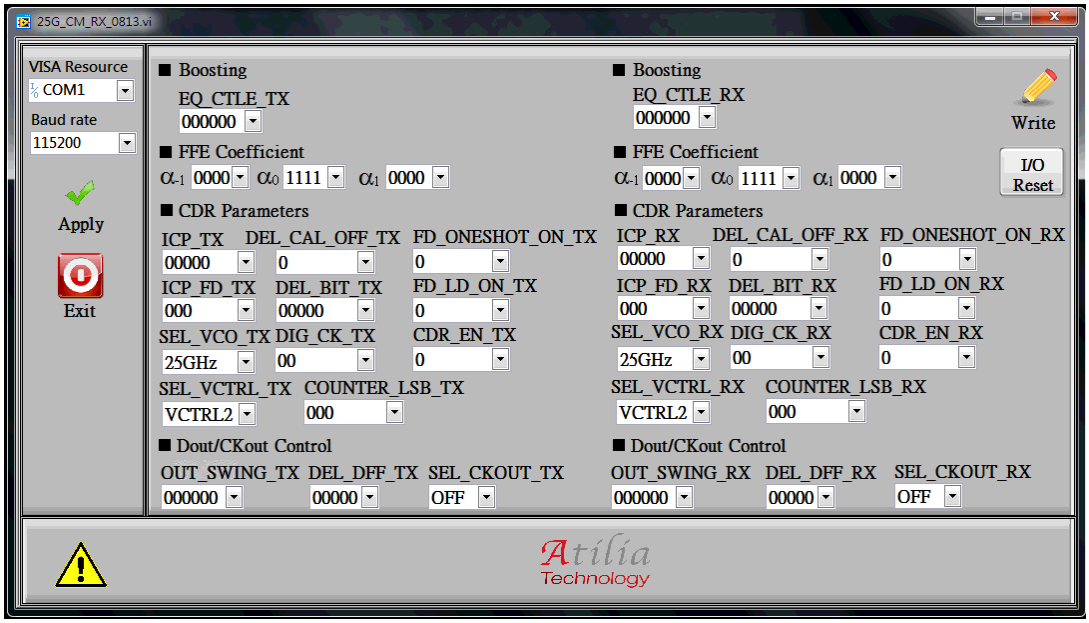

Fig. 7. RX28-NRZ Control Panel.

SYMBOL	RANGE	DESCRIPTION
Boosting		
EQ_CTLE	[000000,111111]	Front-end continuous-time linear equalizer coefficients
FFE Coefficient		
α_{-1}, α_0, α_1	[0000,1111]	3-tap FFE coefficients
CDR Parameters		
ICP	[00000,11111]	Charge pump current DAC
DEL_CAL_OFF	[0,1]	Auto delay calibration activation
FD_ONESHOT_ON	[0,1]	Enabling frequency detection with one-shot signal
ICP_FD	[000,111]	Frequency detection current DAC
DEL_BIT	[00000,11111]	Delay length of retiming clock
FD_LD_ON	[0,1]	Frequency detection lock detector activation
SEL_VCO	[25GHz,28GHz]	Voltage-controlled oscillator operation speed. (25 / 28 GHz)
DIG_CK	[00,11]	Digital clock speed selection
CDR_EN	[0,1]	Enabling CDR or bypassing CDR
SEL_VCTRL	[VCTRL,VCTRL2]	VCO control line selection (FD/PD loop)
COUNTER_LSB	[000,111]	Band counter control LSB
D_{out}/CK_{out} Control		
OUT_SWING	[000000,111111]	Output data voltage swing
DEL_DFF	[00000,11111]	Output data delay length
SEL_CKOUT	[ON,OFF]	Enabling output of generated clock signal

HARDWARE SETUP

Figure 8 shows the front view of **RX28-NRZ EVB**. K connectors are required for connecting both data input and output. Output data should be DC-coupled with proper 50-Ω termination. Input data is AC-coupled and DC-blocks are recommended for input ports. The areas enclosed by the red rectangular lines contain supply voltages and reference voltages required for internal bias generation. Control signal pins in connection with FPGA signals are also included. Labels on the connection wires indicate how each pin is connected to either a power supply or an FPGA control signal port. Make sure the FPGA is powered with its $5V_{DC}$ USB port properly connected to your PC/laptop.

WARNING Please do not apply dc voltages to data output ports. Do not apply input power higher than the recommended value shown in the specifications.

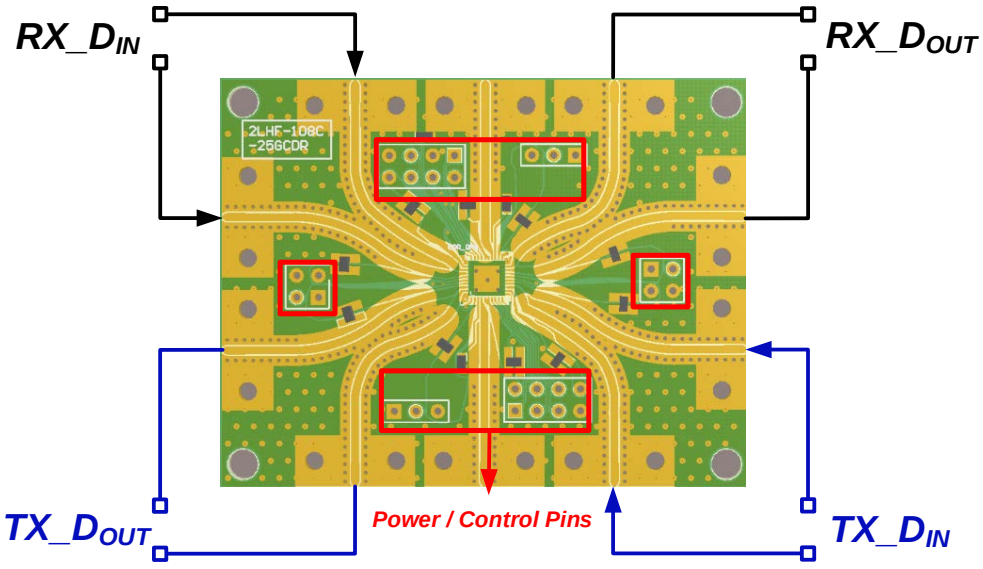

Fig. 8. RX28-NRZ EVB Connection Instruction

OPERATION

RX28-NRZ can be fully controlled by the control software. The following instruction shows an example of detail RX operation.

- Apply input data to the corresponding ports with DC-Blocks. Typical signal generators provide differential RF output. Connect data output to DUT or oscilloscope.
- Connect **RX28-NRZ** to PC's USB port and confirm FPGA module is powered on.
- Activate the control software "Application.exe".
- In the control panel, click on the **USB Port** drop down list box and select **refresh**. Select the proper COM port (i.e., the one assigned in USB driver installation) and clock on **Apply**.
- Set power supply outputs to the labeled values and connect them to the corresponding power pins on EVB. Make sure the input power is within recommended values. Enable outputs of power supply.
- Click **Reset**.
- Use PC interface control panels to adjust **boosting**, **FFE coefficient** and **CDR parameters**. Click **Write**. The **Bypass CDR mode** can be selected by the user. **25GHz/28GHz** modes can also be set.
- Check the waveform on the oscilloscope and try different setup. Whenever the setup is changed, Click **Write** to update.
- **RX28-NRZ** operation and setup example is shown in Fig. 9.

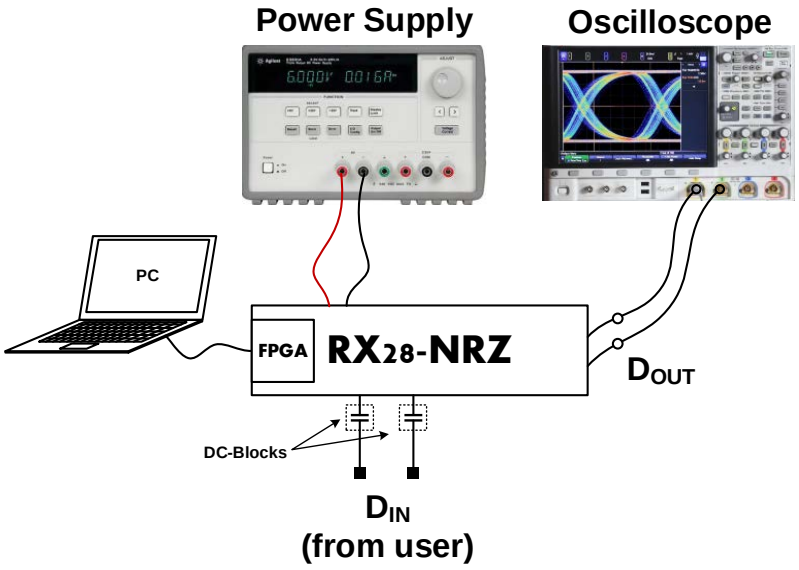

Fig. 9. RX28-NRZ Operation Setup Example. (RX)