Midasmicro

RX28-NRZ

General NRZ receiver 28G

KEY FEATURES

- Wide range input data rate(1~15Gb/s,25,28Gb/s)
- Small input sensitivity < 50 mV (@25Gb/s)
- Wide range programmable output amplitude (300m~930mV_{ppd})
- Output driver with 3-tap FFE provide maximum 8dB boosting
- low power consumption (130mW for Bypass CDR mode,220mW for CDR mode)
- CDR(Clock and Data Recovery circuit) lock time < 10μs
- Supports -20°C to + 100°C temperature range

APPICATIONS

- SerDes and data link testing for 25.78125 Gb/s
- Data center and in-rack connection

DESCRIPTION

The **RX28-NRZ** is a multi-band NRZ receiver with wide input data rate range (1~15Gb/s, 25Gb/s,28Gb/s) and can be applied in typical data link testing. The functional block diagram of RX28-NRZ is shown in Fig. 1, and the CDR architecture is presented in Fig. 2. **RX28-NRZ** can operate in "bypass CDR mode" to save power consumption, in which input data can be operated from 1 to 15Gb/s, and can be only processed by front-end circuits and driven by output driver. When operated in "CDR mode", **RX28-NRZ** can automatically detect input data rate (After select 25Gb/s or 28Gb/s mode) to lock the CDR at correct frequency, and finally recovered differential data output is retrieved with magnitude within 300mV to 930mV (programmable by users, without pre-emphasis), peak-to-peak data jitter less than 7 ps.

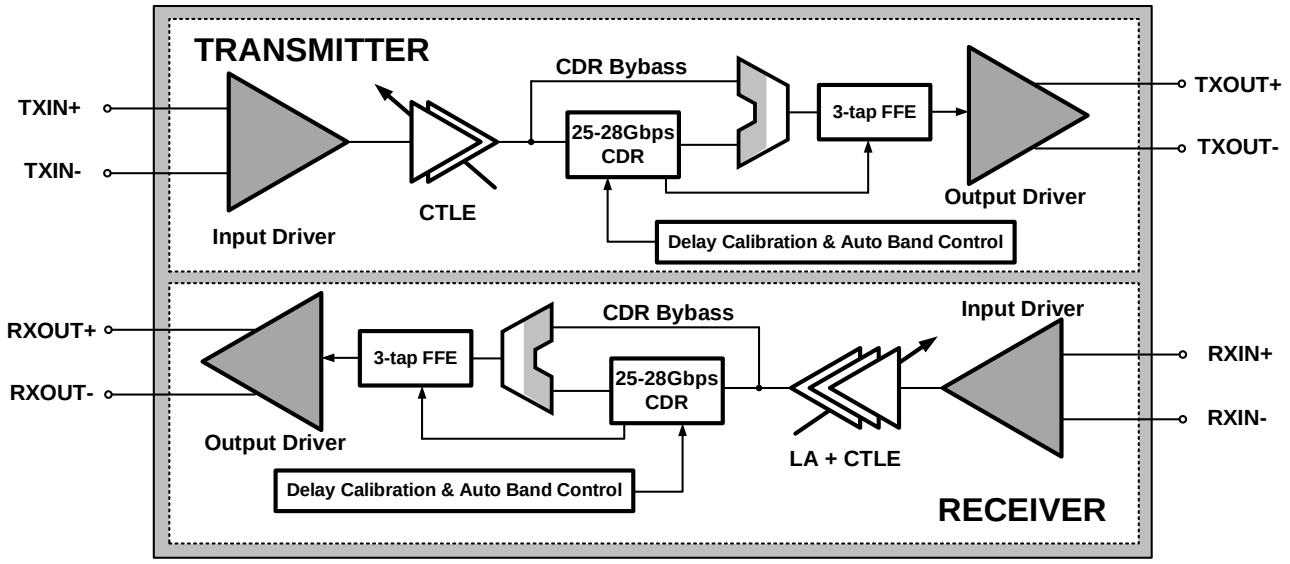


Fig. 1. Functional Block Diagram

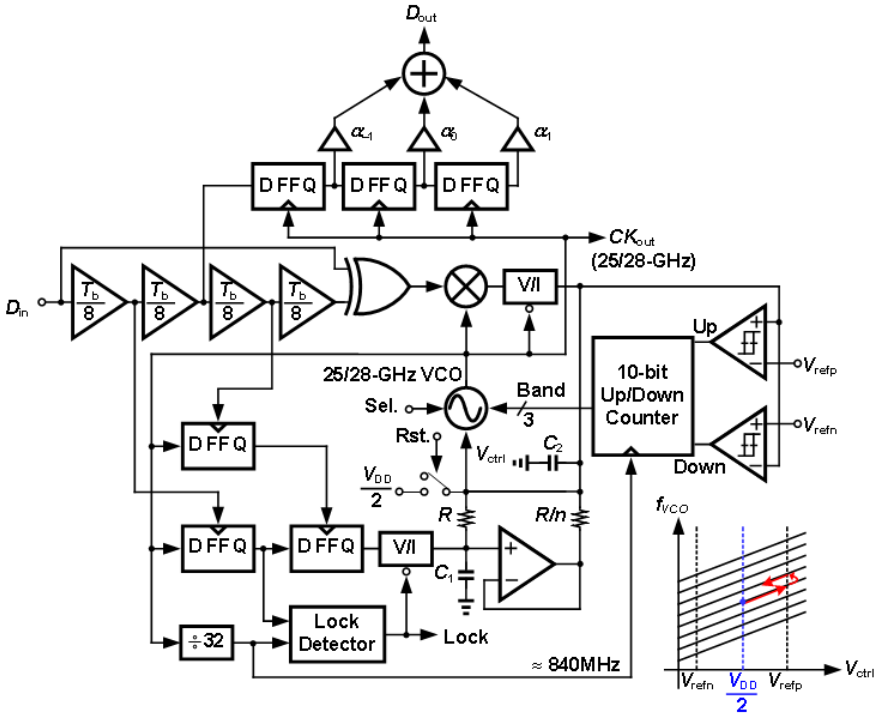


Fig. 2. Clock Data Recovery Architecture

Revision History

Revision	Level	Date	Description
V1	Release	Feb. 2020	Updated footprint drawings example User manual v1 released. (“RX28_NRZ User Manual”)

SPECIFICATIONS

Table 1. Specifications

SYMBOL	PARAMETER	Note	MIN	TYP	MAX	UNIT
RX25-OPT Overall						
VCCR / VCCT	Core supply voltage for RX/TX (CDR/DFE)			1		V
VCCLA	Supply voltage for front-end circuit			1.2		V
VCCDR	Supply voltage for output driver			1.5		V
VCCBG	Supply voltage for bandgap reference			2.5		V
P_{TOTAL}	Power dissipation @ input data rate = 10 Gb/s			130		mW
	Power dissipation @ input data rage = 25 Gb/s			220		mW
Data Input						
DR 25G	Input data rate for bypass CDR mode		1		15	Gb/s
	Input data rate for retime at 25 Gb/s mode		25.5		26	Gb/s
	Input data rate for retime at 28 Gb/s mode		27.5		28.05	Gb/s
V_{in_sense}	Sensitivity at input data rate = 25 Gb/s			50		mV
Data / Clock Output						
V_{OUT_DATA}	Differential data output swing	1	300		930	mV
A_{PRE}	Pre-emphasis, 3-tap FFE, programmable		0		8	dB
$T_{RISE/FALL}$	Output rise/fall time			<13		ps
S_{DD11}	Input differential mode return loss	2		<-10		dB
V_{CM_DATA}	Output data common mode	3	1.035		1.35	V
CDR						
JT_{DATA}	Recovered data jitter @ 25.78125 Gb/s, PRBS31 data			<7.0		ps,pp
				<1.0		ps,rms
JT_{CK}	Recovered clock jitter			<350		fs,rms
T_{LOCK}	CDR lock time			<10		µs
J_{PEAK}	Jitter peaking			<0.1		dB
IJTOL	Input jitter tolerance	4		0.7		UI
RJ	Random jitter w/i CDR			<350		fs,rms
	Random jitter w/o CDR			<1		ps,rms
DJ	Deterministic jitter @ 25 Gb/s			<5		ps,pp
LA & EQ						
A_{LA}	LA gain			20		dB
A_{EQ}	EQ Boosting, programmable		0		9	dB

NOTES:
1. DC-coupled, 50-Ω terminated, 1.85mm female (CML Logic).
2. From 0.01 GHz to 28 GHz
3. Single-ended, DC-coupled, 50-Ω terminated
4. SJ=0.2UI, High-frequency JTOL > 0.2 UI

Measured Output Data Waveforms

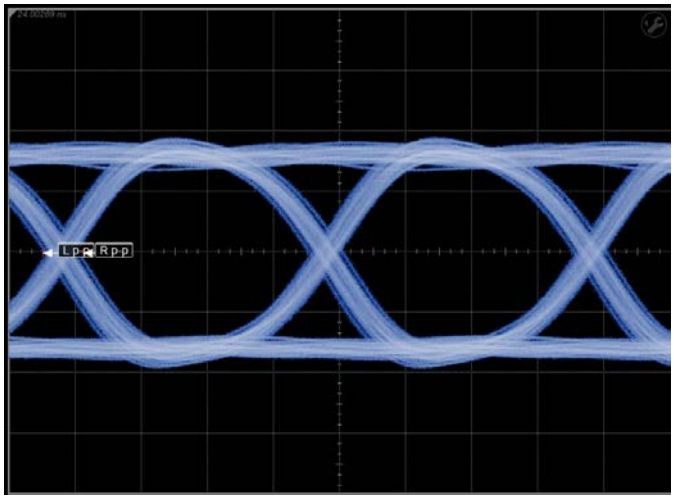


Fig. 3. Output Data Eye at 25 Gb/s, PRBS7

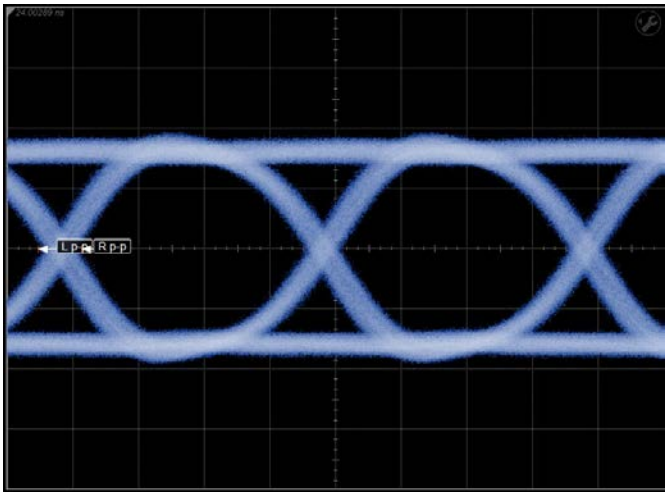


Fig. 4. Output Data Eye at 25 Gb/s, PRBS15

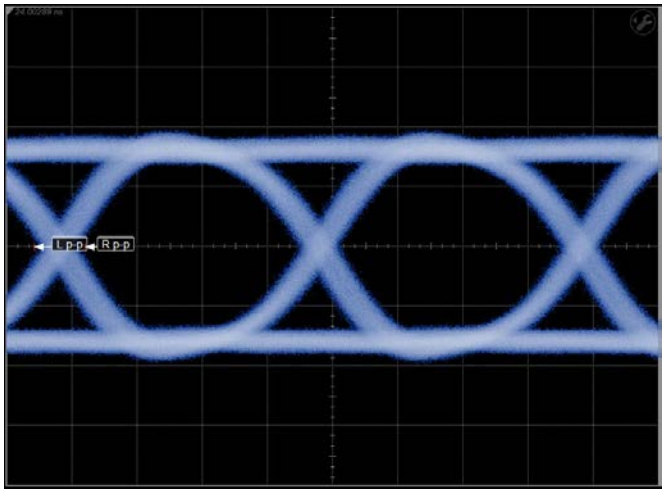


Fig. 5. Output Data Eye at 25 Gb/s, PRBS23

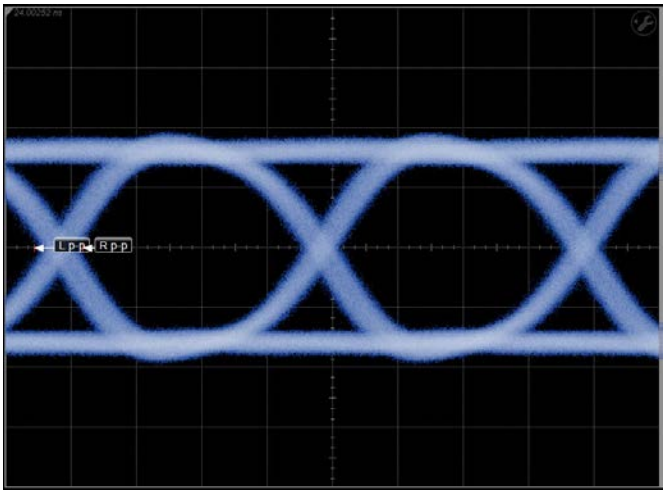


Fig. 6. Output Data Eye at 25 Gb/s, PRBS31

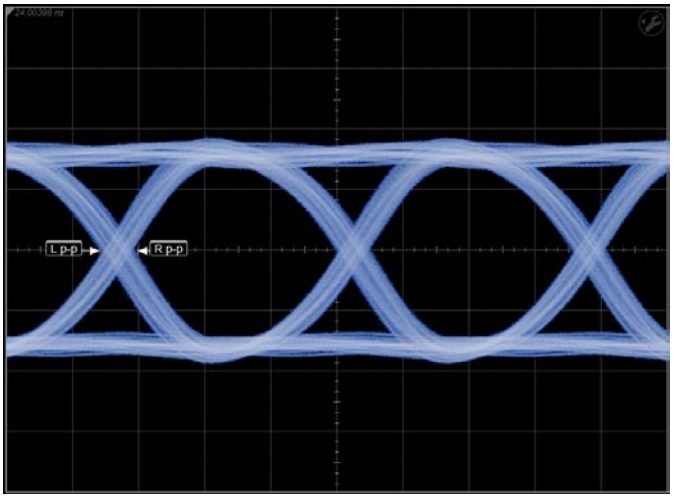


Fig. 7. Output Data Eye at 28 Gb/s, PRBS7

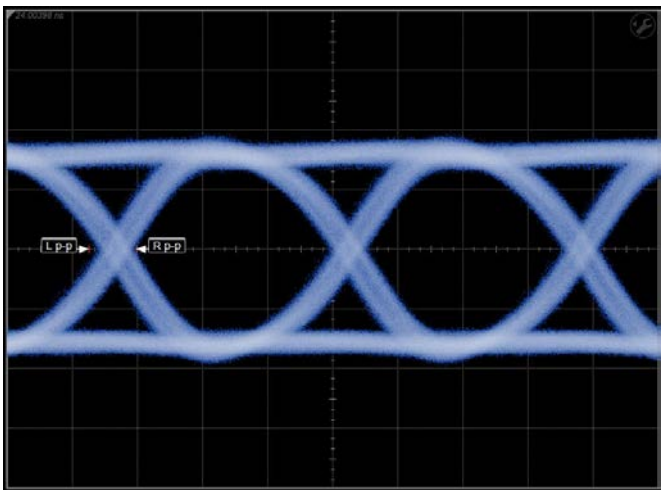


Fig. 8. Output Data Eye at 28 Gb/s, PRBS15

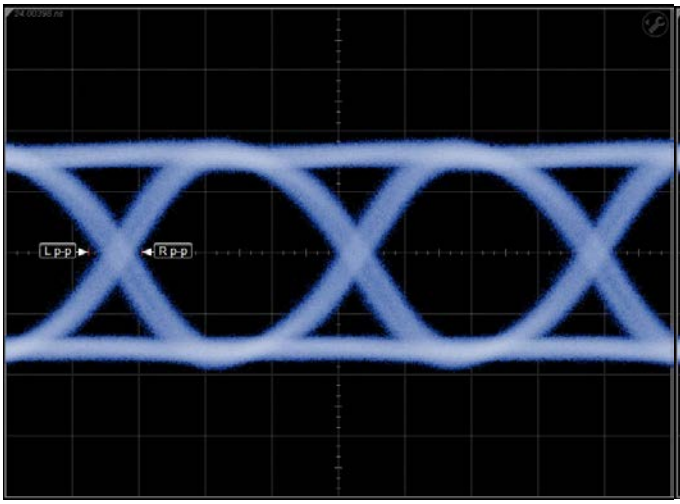


Fig. 9. Output Data Eye at 28 Gb/s, PRBS23

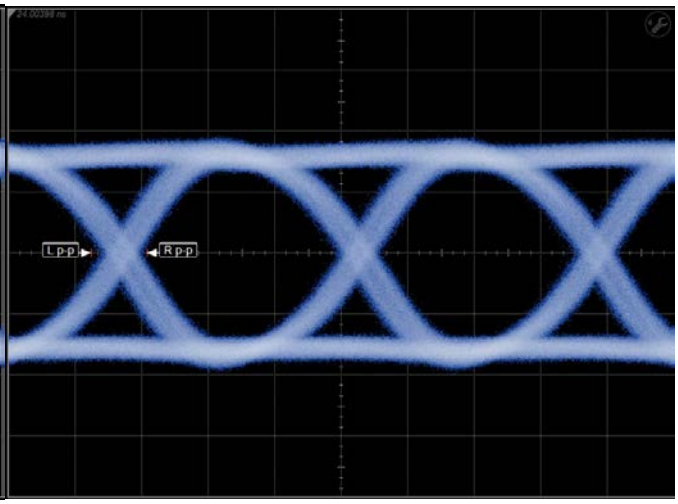


Fig. 10. Output Data Eye at 28 Gb/s, PRBS31

Data Jitter Summary (with 5-cm RO4003 Trace)

The data jitter measurement is presented as below. The jitter specifications are marked in the picture and are summarized on the specification table.

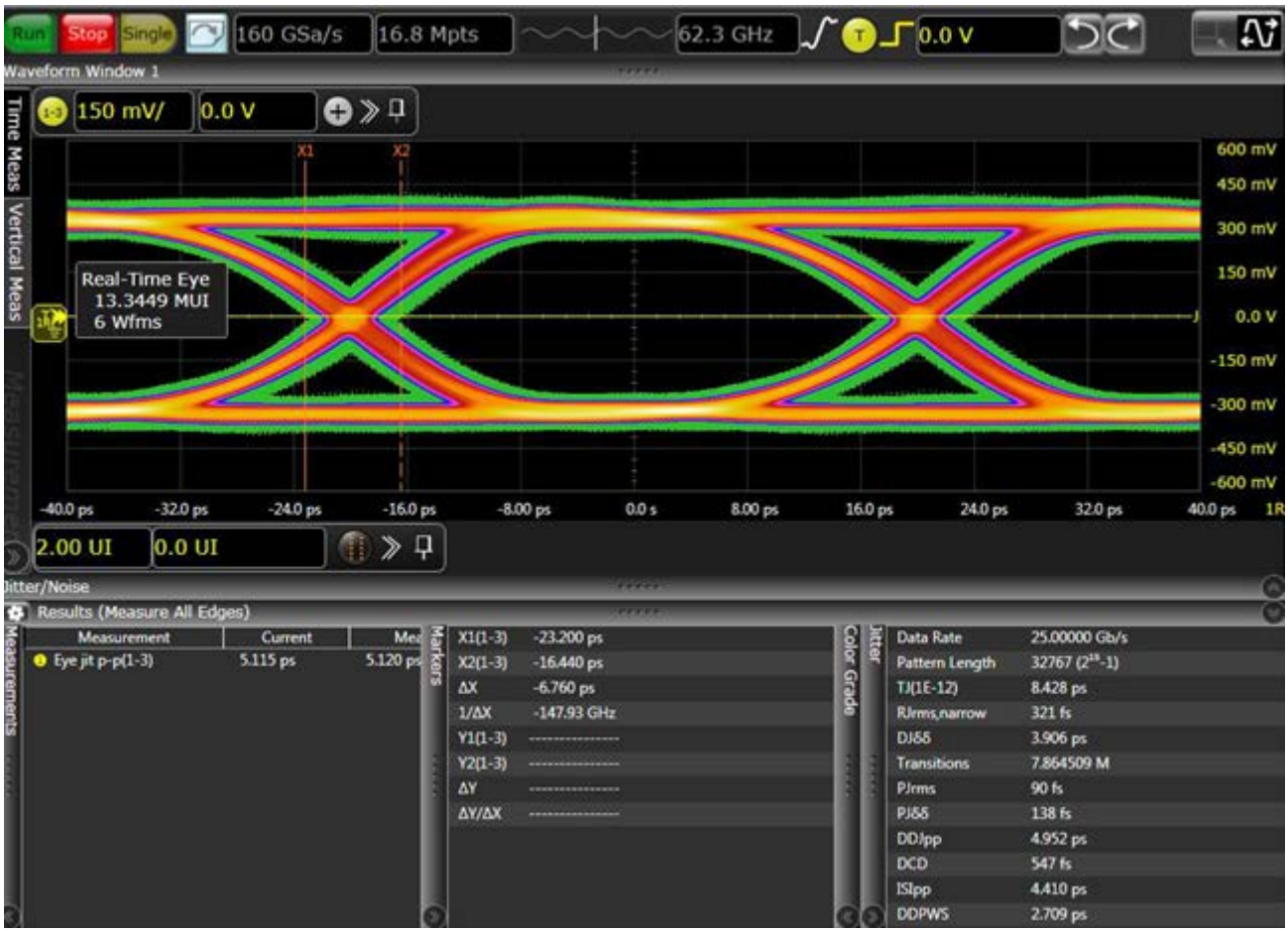


Fig. 11. Data Jitter Summary

Jitter Tolerance Measurement (with 5-cm RO4003 Trace)

The measurement of sinusoidal jitter tolerance is presented as below. High-frequency JTOL is better than 0.2 UI.

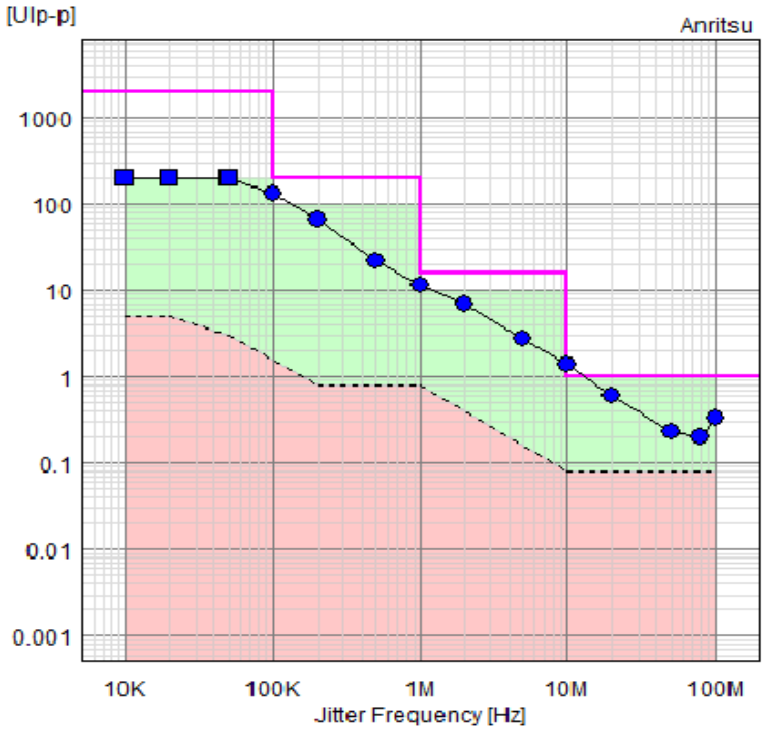


Fig. 12. Jitter Tolerance

CHIP PHOTO & PIN CONFIGURATION

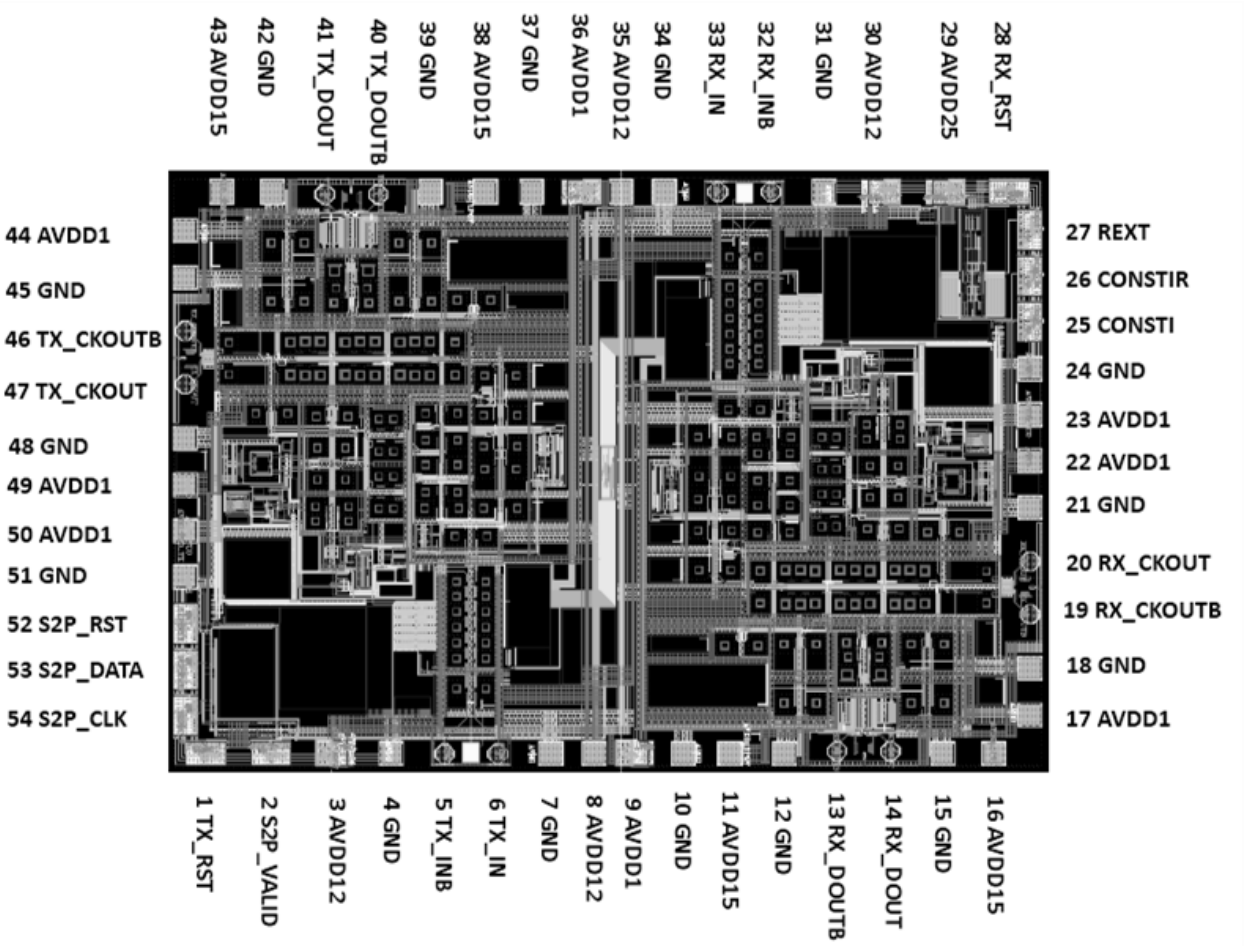


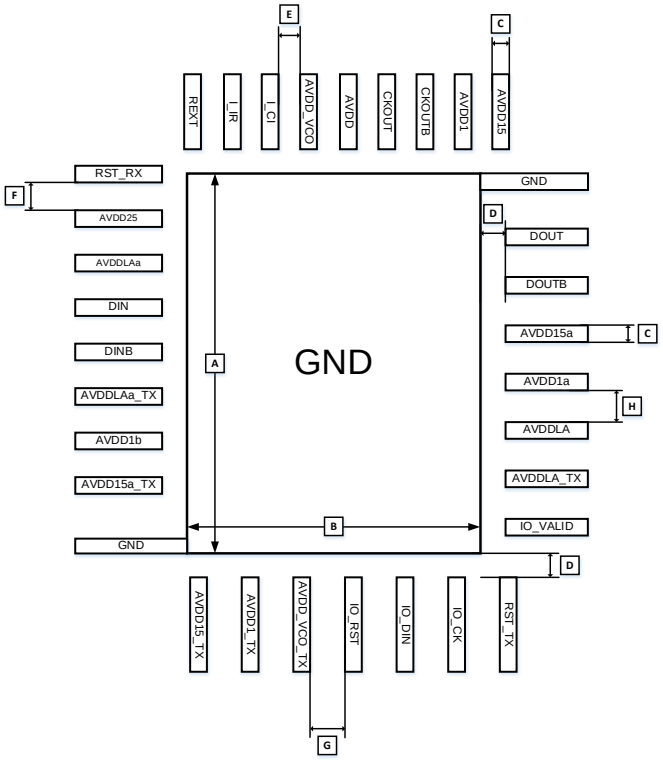
Fig. 13. Pin Configuration

Pin Function Descriptions

Table. 2. Pin Function Descriptions

Pin No.	Pin Name	Type	Description
1	TX_RST	Analog Input	The reset of TX CDR.
2	S2P_VALID	Analog Input	The valid of Serial Peripheral Interface.
3, 8, 30, 35	AVDD12	Power	Positive power supply for the front-end circuit. Typical value is 1.2V.
4, 7, 10, 12, 15, 18, 21, 24, 31, 34, 37, 39, 42, 45, 48, 51	GND	Ground	Analog ground.
5, 6	TX_INB, TX_IN	CML Input	The TX differential data input.
9, 17, 22, 23, 36, 44, 49, 50	AVDD1	Power	Positive power supply for the CDR. Typical value is 1V.
11, 16, 38, 43	AVDD15	Power	Positive power supply for the output driver Typical value is 1.5V.
13, 14	RX_DOUTB, RX_DOUT	CML Output	RX Recovered differential full-rate data output.
19, 20	RX_CKOUTB, RX_CKOUT	CML Output	RX Recovered differential full-rate clock output.
25	CONSTI	Analog Input	Bias of constant current.
26	CONSTIR	Analog Input	Bias of constant IR drop.
27	REXT	Analog I/O	Connecting a resistor between this pin and ground.
28	RX_RST	Analog Input	The reset of RX CDR.
29	AVDD25	Power	Positive power supply for the high to low circuit and bandgap reference. Typical value is 2.5V.
32, 33	RX_INB, RX_IN	CML Input	The RX differential data input.
40, 41	TX_DOUTB, TX_DOUT	CML Output	TX Recovered differential full-rate data output.
46, 47	TX_CKOUTB, TX_CKOUT	CML Output	TX Recovered differential full-rate clock output.
52	S2P_RST	Analog Input	The reset of Serial Peripheral Interface.
53	S2P_DATA	Analog Input	The data input of Serial Peripheral Interface.
54	S2P_CLK	Analog Input	The clock input of Serial Peripheral Interface.

Recommended Footprint Example for Testing RX28-NRZ Receiver (wire bonding)



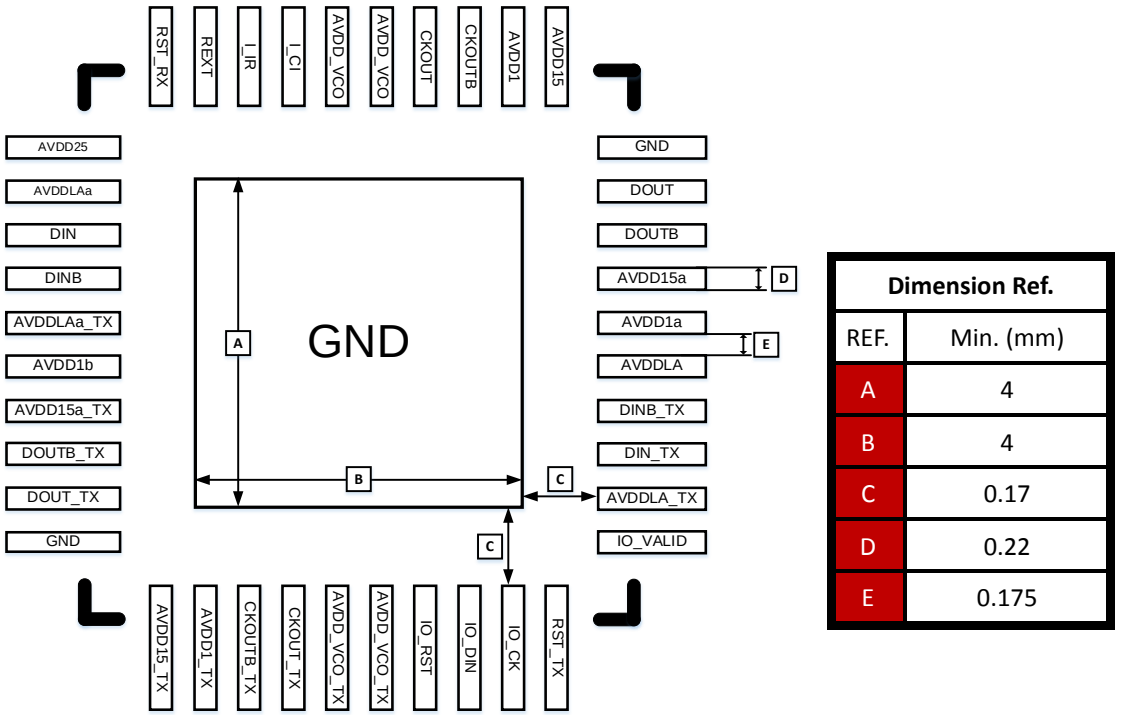
Dimension Ref.	
REF.	Min. (mm)
A	1.2
B	1.8
C	0.12
D	0.164
E	0.12
F	0.12
G	0.14
H	0.195

Fig. 14. Recommended Footprint Example for Wire Bonding

Table. 3. Footprint Mapping to Chip Pins (1)

Footprint Name	Pin Name	Footprint Name	Pin Name	Footprint Name	Pin Name
REXT	REXT	*AVDDLA_TX*	AVDD12	*DIN*	RX_IN
I_IR	CONSTIR	*IO_VALID*	S2P_VALID	*AVDDLAa*	AVDD12
I_CI	CONSTI	*RST_TX*	TX_RST	*AVDD25*	AVDD25
AVDD_VCO	AVDD1	*IO_CK*	S2P_CLK	*RST_RX*	RX_RST
AVDD	AVDD1	*IO_DIN*	S2P_DATA		
CKOUT	RX_CKOUT	*IO_RST*	S2P_RST		
CKOUTB	RX_CKOUTB	*AVDD_VCO_TX*	AVDD1		
AVDD1	AVDD1	*AVDD1_TX*	AVDD1		
AVDD15	AVDD15	*AVDD15_TX*	AVDD15		
GND	GND	*GND*	GND		
DOUT	RX_DOUT	*AVDD15a_TX*	AVDD15		
DOUTB	RX_DOUTB	*AVDD1b*	AVDD1		
AVDD15a	AVDD15	*AVDDLAa_TX*	AVDD12		
AVDD1a	AVDD1	*DINB*	RX_INB		

Recommended Footprint Example for Testing RX28-NRZ Transceiver (QFN 5x5 Package)



Dimension Ref.	
REF.	Min. (mm)
A	4
B	4
C	0.17
D	0.22
E	0.175

Fig. 15. Recommended Footprint Example for QFN Package

Table. 4. Footprint Mapping to Chip Pins (2)

Footprint Name	Pin Name	Footprint Name	Pin Name	Footprint Name	Pin Name
RST_RX	RX_RST	*AVDD1a*	AVDD1	*AVDD15_TX*	AVDD15
REXT	REXT	*AVDDLA*	AVDD12	*GND*	GND
I_IR	CONSTIR	*DINB_TX*	TX_IN	*DOUT_TX*	TX_DOUT
I_CI	CONSTI	*DIN_TX*	TX_INB	*DOUTB_TX*	TX_DOUTB
AVDD_VCO	AVDD1	*AVDDLA_TX*	AVDD12	*AVDD15a_TX*	AVDD15
AVDD	AVDD1	*IO_VALID*	S2P_VALID	*AVDD1b*	AVDD1
CKOUT	RX_CKOUT	*RST_TX*	TX_RST	*AVDDLAa_TX*	AVDD12
CKOUTB	RX_CKOUTB	*IO_CK*	S2P_CLK	*DINB*	RX_INB
AVDD1	AVDD1	*IO_DIN*	S2P_DATA	*DIN*	RX_IN
AVDD15	AVDD15	*IO_RST*	S2P_RST	*AVDDLAa*	AVDD12
GND	GND	*AVDD_VCO_TX*	AVDD1	*AVDD25*	AVDD25
DOUT	RX_DOUT	*CKOUT_TX*	TX_CKOUT		
DOUTB	RX_DOUTB	*CKOUTB_TX*	TX_CKOUTB		
AVDD15a	AVDD15	*AVDD1_TX*	AVDD1		

Notes on the RX28-NRZ PCB Footprint

The RX28-NRZ is compatible with both Chip-on-Board (COB) and QFN packages. The size of package for QFN is 5x5, 40 pins. The PCB trace mappings to the pins of RX28-NRZ are described in P.12.

System Function Descriptions

1. Linear CDR

The system adopts full-rate clock and data recovery circuit (CDR), which employs a mixer-type linear phase detector and an automatic frequency locking technique. The phase detector achieves high-speed operation by mixing the clock with the data-transition pulses, providing outputs proportional to the phase error. The frequency acquisition loop utilizes the data phases rather than the clock phases to distill the frequency difference, and no external reference is required in this design. For data rate ranges from 25-Gbps to 28-Gbps, CDR can be activated for regular operation. Under low-speed condition for data rate from 1-Gbps to 15-Gbps, CDR can be bypassed by user control.

2. Frontend Limiting Amplifier and CTLE

The receiving channel includes a high-sensitivity limiting amplifier and a continuous-time linear equalizer (CTLE). CTLE is programmed externally by controlling the DAC to adjust the boosting range according to different levels of channel loss.

3. Data Output Pre-emphasis

Data output can be de-emphasized by 3-tap feed-forward equalizer (FFE) to compensate channel loss. Three taps of FFE include main-tap, pre-tap, and post-tap, respectively. The maximum boosting is up to 8dB.

4. Delay Calibration

As the function block diagram shown in Fig. 1, the system employs linear CDR architecture which requires two delay cells to generate quadrature unit interval delay. At the initial state of system, the delay is not the correct value for linear CDR operation. A delay calibration scheme is built in the CDR which adaptively adjusts the delay to fit correct CDR operation.

5. Auto VCO band lock

The voltage-controlled oscillator (VCO) is designed to cover the range of operating data rate. Note that one single band is not wide enough to cover the complete range of operating data rate due to the trade-off between K_{VCO} and phase noise performance. Multiple frequency band is implemented in single VCO by switching the capacitor bank array. The oscillation frequency is modified by the constant inductance and variable capacitance. At initial state, the VCO oscillation frequency may be deviated from the correct frequency needed for resampling the input data, and the required frequency does not necessarily lie within the correct frequency band of VCO. Therefore, an auto

VCO band lock scheme is embedded to trace the data rate and dynamically change the frequency band.

6. Output swing control

System is equipped with programmable output swing which can be programed by external interface. The output swing can be controlled by changing the current using programmable DAC.